MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

type A2A(S1)/A3ACPU-F (SUPPLEMENT)

MITSUBISHI ELECTRIC

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

1. GENERAL DESCRIPTION

This manual explains the CPU performance specifications, necessary peripheral devices, and programming precautions to take when operating an A2ACPU-F, A2ACPU-S1-F, or A3ACPU-F PC (all hereafter called an AnACPU-F) using SFC language.

With an AnACPU-F, SFC processing time is considerably faster than with an AnNCPU-F (A1SCPU, A0J2HCPU, and A2CCPU are included).
The AnACPU has been designed to increase the ladder processing speed. However, the SFC processing time is longer than the processing time required for a ladder processing only.

1.1 Features

(1) The SFC system processing time has been shortened
When operating an SFC program, system processing time is necessary as an overhead. However, this time was reduced. Therefore, as compared with an AnACPU-F, the total scan time has been reduced.

(2) A block single start functions for an inactive block has been added
A function that singly starts an inactive block by using either a sequence program or a peripheral device has been added. This makes both partial testing of equipment and debugging of SFC programs easier.

1.2 Use with Related Manuals

This manual gives the precautions to take and the specifications of the MELSAP-II function (SFC) which is necessary to operate an AnACPU-F using SFC language.
When consulting the related manuals given below, read the indicated sections as if they were contents of this manual.

Related manuals:

(1) MELSAP-II Programming Manual (IB(NA)66361)
- Applicable CPU (see Section 2.1)
- Configuration of the user memory area (see Section 2.2)
- List of devices (see Section 3.2)
- SFC program processing time (see Section 3.3)
- Instructions used for operation output/transition conditions (see Sections 4.3 and 4.6)
- List of error codes (see Section 8)

(2) SW0IX-SAP2E (MELSAP-II) Operating Manual (IB(NA)66313)
- Applicable CPU (see Section 2.1)
- Inactive block single start (newly-added function)

(3) SW0IX-GPPAE GPP Function Operating Manual (IB(NA)66314)
- Parameter memory capacity setting (see Section 7.2)
- Precautions to take when setting the microcomputer program capacity for an AnACPU (newly-added function)

(4) A2A(S1)/A3ACPU User's Manual (Control Functions) (IB(NA)66256)
- CPU module performance specifications (see Section 3.1)
- User memory allocation (see Section 5.1.2)
- Changing LED display priorities (see Section 3.16)

(5) The User's Manual of each special module that can read/write a sequence program
- Microcomputer program read/write suitability (see the section in each particular manual that explains the commands)

2. COMPATIBLE PERIPHERAL DEVICES AND SOFTWARE PACKAGES

Table 2.1 shows the peripheral devices that can and cannot be used for creating and debugging SFC programs when operating an AnACPU-F using the SFC language during monitoring, as well as the software packages for the GPP and SFC functions.

Table 2.1 Combinations of Compatible Peripheral Devices and Software Packages

Peripheral Devices	GPP Function Software Packages	MELSAP-II (SFC) Function Software Packages	Combinable
*1 A7PHPE	*1 SW0RX-GPPAE	*1 SW0RX-SAP2E	OK
PC/AT or compatible	*2 SW0IX-GPPAE	SW0IX-SAP2E, Version B or earlier	NG
		SW0IX-SAP2E, Version C or later	OK

POINTS

(1) *1: Available as of July, 1992.
*2: There are no restrictions on which SW0IX-GPPAE GPP function software package can be combined with the MELSAP-II(SFC) function software package SW0IX-SAP2E.

(2) The SW4GP-GPPA GPP function software package for an A6GPP/A6PHP is version E or later. If the version is E or later, there is an additional function about microcomputer program capacity setting in the memory capacity setting option of parameter setting for an AnA-F.
SFC programs cannot be created and displayed. Memory contents can be confirmed and changed. Microcomputer programs (SFC programs) can be read/written from/to the CPU and a floppy disk.

3. CPU MODULE PERFORMANCE SPECIFICATIONS

This section indicates how the performance specifications of an AnACPU-F differ from those of an AnACPU.
Any specifications not given in this section are the same for both an AnACPU-F and an AnACPU.
The A2A(S1)/A3ACPU User's Manual (Control Function) gives details.

Items	A2A/A2ACPU-S1-F	A3ACPU-F
Available memory cassette	A3NMCA-0 *1 ~ A3NMCA-56	A3NMCA-0 *1 ~ A3NMCA-56 A3AMCA-96
Main program capacity	Sequence program + microcomputer program * 2 = max. 14 Ksteps (28 Kbytes) Microcomputer program = max. 13 Ksteps (26 Kbytes) can be set.	Sequence program + microcomputer program * 2 = max. 30 Ksteps (60 Kbytes) Microcomputer program = max. 29 Ksteps (58 Kbytes) can be set.
Sub-program capacity	No function.	Sequence program = max. 30 Ksteps can be set. (Microcomputer programs cannot be set.)

*1: Since work areas for an SFC program cannot be allocated in an A3MCA-0 or A3NMCA-0, an A3MCA-0 and A3NMCA-0 cannot be utilized.
*2: Since the microcomputer program area can only be used for storing SFC programs, the microcomputer program area cannot be used for storing microcomputer programs created by a user.
In addition, the microcomputer program area cannot be used as an additional area for utility software packages for the MELSEC-A series.

4. USER MEMORY WHEN EXECUTING AN SFC PROGRAM

This section explains the relationship between user memory areas in an SFC program work area and memory cassettes needed to execute SFC programs.

4.1 Memory Area Allocations for Memory Cassette Users

Table 4.1 shows the memory area allocations for memory cassette users when doing parameter setting.

Table 4.1 Memory Area Allocations for Memory Cassette Users

ROM memory area	Unusable		
	Parameter area		... 3 Kbytes (indespensible)
	T/C set value area (main program use)		... 1 Kbytes (indispensable)
*4 2)	Main sequence program area	Sequence area	... Set parameters in the range of 1 to 30 Ksteps (2 to 60 Kbytes).
		Microcomputer area	... Set parameters in the range of 2 to 58 Kbytes (However, it can be set within 60 Kbytes with a sequence area.)
*5 1)	T/C set value area (sub-program use)		... 1 Kbyte (When a sub-program is set)
3)	Sub-sequence program area		... Set parameters in the range of 0 to 30 Ksteps (0 to 60 Kbytes). (Settings can only be done with an A3A-F.)
*5 RAM memory area	System area for sub-sequence execution		... 5 Kbytes (When a sub-program is set)
4)	Extension comment area		... When a capacity is set using a parameter * 1
	Extension file register	Block No. 8	... One block = 16 Kbytes *2/*3 max. 8 blocks
		≀	
		Block No. 2	
		Block No. 1	
	File register area		... Set parameters in the range of 0 to 16 Kbytes.
5)	Comment area		... Set parameters in the range of 0 and 2 to 64 Kbytes.
	Extension file register	Block No. □	... 1 block = 16 Kbytes With an A2A(S1) : □=28 With an A3A : □=48
		≀	
		Block No. 10	

*1: If the extension comment capacity > {1)–2)–3)–5) Kbytes} when setting an extension comment. Extension comments are stored after block No. 10 of the extension file register.
If an extension comment is stored in block No. 10, area 4) is the available area for calculating the number of blocks of extension file registers of block Nos. 1 to 8.
If the block area after No. 10 is smaller than the set extension comment capacity, the memory area will be insufficient. Therefore, CPU write operations cannot be done.

*2: Calculate the available number of blocks of an extension file register (block Nos. 1 to 8)

- During RAM operation $\frac{1) - 2) - 3) - (4)) - 5) \text{ K bytes}}{16} = n1$
- During ROM operation $\frac{1) - 3) - (4)) - 5) \text{ Kbytes}}{16} = n2$

The integer value of n1 and n2 is the available number of blocks in block numbers 1 to 8.

*3: Designate an extension file register block number to the data storage area numbers of a sampling trace and a status latch when a sampling trace and status latch are being executed online.

*4: This area can be stored to the ROM.
When this area is stored to the ROM, areas 3) and 4) are condensed. And then, the size of an available area for calculating the number of available blocks of extension file registers of block numbers 1 to 8 increases.

*5: The following table gives the capacities of each memory cassette model.

Memory Cassette Model Names	Memory Cassette Capacities	Capacities in Table 4.1 (1)
A3(N)MCA-0	—	—
A3(N)MCA-2	16 Kbytes	16 Kbytes
A3(N)MCA-4	32 Kbytes	32 Kbytes
A3(N)MCA-8	64 Kbytes	64 Kbytes
A3MCA-12	96 Kbytes	96 Kbytes
A3NMCA-16	128 Kbytes	96 Kbytes
A3MCA-18	144 Kbytes	144 Kbytes
A3NMCA-24	192 Kbytes	144 Kbytes
A3NMCA-40	320 Kbytes	144 Kbytes
A3NMCA-56	448 Kbytes	144 Kbytes
A3NMCA-96 (only for an A3A(-F))	768 Kbytes	144 Kbytes

4.2 SFC Program Work Area and Step Trace Data Storage Area

(1) SFC program work area
When executing an SFC program, the system uses 4 Kbytes of the user memory area of a memory cassette as an SFC program work area. In addition, the system uses a max. 12 Kbytes as the step trace data storage area.
If the user memory area of a memory cassette does not have an available capacity of 4 Kbytes or more, SFC programs cannot be executed.
When executing a step trace, 2 to 12 Kbytes of available area are necessary in addition to the 4 Kbytes for the work area.

(2) How to calculate the available capacity of a memory cassette's user memory area
The available capacity is calculated by subtracting the parameter-set memory capacity from the total area that can be parameter-set.
Max. 144 Kbytes (Area indicated in Table 4.1 (1))

Sample calculation: The following shows a sample calculation of an available capacity when the following conditions have been satisfied.

Memory cassette.....A3NMCA-24
Main program
(microcomputer program included).....10 Ksteps
File register.....4 Kpoints
Comment.....40 Kbytes

Memory space capacity =

144 K – (3 K + 1 K + 20 K + 8 K + 40 K) = 72 Kbytes
1) 2) 3) 4) 5) 6)

1): Capacity of an A3NMCA-24 that can be parameter-set (Area indicated in Table 4.1(1))
2): Parameter storage area
3): T/C set value area
4): Main program (1 step 2 bytes = 10 Ksteps x 2)
5): File register (1 point 2 bytes = 4 Kpoints x 2)
6): Comment capacity

The memory space capacity is calculated as 72 Kbytes.

4.3 How to Calculate the Area Capacity Used as an SFC Program Work Area

This section shows how to calculate the area capacity of the memory cassette that is used as an SFC program work area and whether or not an SFC program can be executed.
When an SFC program cannot be executed in the following explanation, it is necessary to change either (a) the memory cassette, or (b) the memory capacity parameter setting.
The memory capacity set with a parameter in the following explanation is the sum of the memory capacity when a user set or changed the memory capacity set with parameters.
The default value is 16 Kbytes.

(1) If the memory cassette is one of the following:
- A3(N)MCA-2
- A3(N)MCA-4
- A3(N)MCA-8
- A3MCA-12

(Area capacity of Table 4.1(1))
– (Memory capacity set with a parameter) = A

A : 16 Kbytes or more
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 1 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.
: More than 4 Kbytes less than 15 Kbytes
.....an SFC program can be executed.
Step trace capacity ≤ A – 4 Kbytes.
: 4 Kbytes or less
.....an SFC program cannot be executed.

(2) If the memory cassette is the following:
- A3NMCA-16

(Area capacity of Table 4.1 (1))
– (Memory capacity set with a parameter) = A

* When an extension comment capacity is set, and A is minus
(Area capacity of Table 4.1 (1)) –
(Memory capacity set with a parameter – extension comment capacity) = B

A : 16 Kbytes or more
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 1 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.
: 15 Kbytes or less
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
However, the work area is moved to extension file register No. 10.
Since extension file register No. 10 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.

B : 16 Kbytes or more
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 1 is utilized as a SFC program work area, this cannot be utilized as an area for user data storage.
: More than 4 Kbytes and less than 15 Kbytes
.....an SFC program can be executed.
Step trace capacity ≤ B – 4 Kbytes.
: 4 Kbytes or less
.....an SFC program cannot be executed.

(3) If the memory cassette type is the following:
- A3NMCA-18

(Area capacity of Table 4.1 (1))
– (Memory capacity set with a parameter) = A

A : 32 Kbytes or less
.....an SFC program can be executed and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 2 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.
: More than 4 Kbytes less than 15 Kbytes
.....an SFC program can be executed.
Step trace capacity ≤ A – 4 Kbytes.
: More than 16 Kbytes and less than 31 Kbytes
.....an SFC program cannot be executed.
However, an SFC program can be executed by parameter setting of a dummy capacity and setting the capacity of "A" at 15 Kbytes or less.
: 4 Kbytes or less
.....an SFC program cannot be executed.

(4) If the memory cassette is one of the following:
- A3NMCA-24
- A3NMCA-40
- A3NMCA-56
- A3NMCA-96

(Area capacity of Table 4.1(1))
– (Memory capacity set with a parameter) = A

* When an extension comment capacity is set, and A is minus
(Area capacity of Table 4.1 (1)) –
(Memory capacity set with a parameter – extension comment capacity) = B

A : 32 Kbytes or more
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 2 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.
: 15 Kbytes or less
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
However, the work area is moved to extension file register No. 10.
Since extension file register No. 10 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.

B : 32 Kbytes or lees
.....an SFC program can be executed, and a max. 12 Kbytes step trace capacity can be occupied.
Since extension file register No. 2 is utilized as an SFC program work area, this cannot be utilized as an area for user data storage.
: More than 4 Kbytes and less than 15 Kbytes
.....an SFC program can be executed.
Step trace capacity ≤ B – 4 Kbytes.
: More than 16 Kbytes and less than 31 Kbytes
.....an SFC program cannot be executed.
However, an SFC program can be executed by parameter setting of a dummy capacity and setting the capacity of "A" at 15 Kbytes or less.
: 4 Kbytes or less
.....an SFC program cannot be executed.

4.4 Functions Using an Extension File Register and Area Occupation Timing

Table 4.3 shows the functions using an extension file register, area occupation timing, and area occupation priorities.

Table 4.3 Functions Using an Extension File Register and Area Occupation Timing

Functions Using an Extension File Register	Area Occupation Timing	Area Occupation Priority
Extension comment	When a parameter with which an extension comment capacity was set is written to a CPU	1
SFC work area	When a parameter with which a microcomputer program capacity was set is written to a CPU	2
Online sampling trace Online status latch	When trace/latch data storage register No. is set and is written to a CPU	3
Extension file register access instruction Access by a computer link	When an instruction is executed or when a computer link is accessed Presence or absence of the corresponding block numbers and access validity are checked at this time	4

*1: If the memory capacity of a parameter is changed after executing an SFC program, block No. 10 of an SFC program work area sometimes changes. Sections 4.1 and 4.2 give details about confirming the block number that is used as a work area.

*2: If an SFC program is designated to the continuation start and a program is started when a parameter is first written to a CPU or when the memory capacity of a parameter is changed, SFC PARA.ERROR (error code 80 and detailed error code 804) occur. And then, an SFC program is started from the initial step of block 0.

5. PROGRAMMING PRECAUTIONS

This section gives the precautions to take when programming to execute an SFC program on an AnA-F.

5.1 To Execute an SFC Program by Continuation Restart

(1) To execute an SFC program by contunuation restart on an AnA-F, special relay M9102 must be turned ON (contunuation restart) all the time an SFC program is being executed.
If M9102 is turned ON when an SFC program is restarted, after it is executed with M9102 being turned OFF, the SFC PARA. ERROR (error code 80, detail error code 804) message is displayed. Then, an SFC program is started by initial start (start with the initial step in block 0).

(2) When an SFC program is executed, the SFC processing time of the CPU varies according to the ON/OFF status changes of M9102.
The list of processing times in Section 7.2 gives details.

5.2 Instructions and Devices Usable as Operating Outputs and Transition Conditions

(1) Instructions usable as operating outputs

(a) Common instructions except for the following are usable:
CJ, SCJ, JMP, FEND, RET, IRET, MC, MCR, CHG, CHK, and labels Pn and In

(b) Dedicated instructions except for the following are usable:
BREAK, CHK, and CHKEND

(2) Instructions usable as transition conditions

- Contact instructions:
  LD, LDI, AND, ANI, OR, ORI
- Branch end instructions:
  ANB, ORB
- Comparison operation instructions:

LD(D)=	, LD(D)>	, LD(D)>=	, LD(D)<>
LD(D)<	, LD(D)<=	,	
AND(D)=	, AND(D)>	, AND(D)>=	, AND(D)<>
AND(D)<	, AND(D)<=	,	
OR(D)=	, OR(D)>	, OR(D)>=	, OR(D)<>
OR(D)<	, OR(D)<=		

(3) Devices usable with an SFC program
Extension devices (M2048 to 8191, D1024 to 6143, etc.) of an AnACPU can be utilized in the ladder circuits of operating outputs and transition conditions, and for SFC data registers when used with an SFC program.

5.3 Microcomputer Program Area of an AnACPU-F

(1) Using a microcomputer program with an AnACPU-F
The microcomputer program area of an AnACPU-F can be utilized for storing an SFC program.
This area cannot be utilized for storing a user's microcomputer programs or as an additional area for a utility software package for the MELSEC-A series.

(2) Precautions when writing a parameter to a CPU when the parameter has been set with a microcomputer program capacity
If an attempt is made to write a parameter with which a microcomputer program capacity has been set to an AnACPU which does not have the -F code, a parameter error occurs which disables the CPU.
Do not set a microcomputer program capacity with a parameter on a peripheral device except when an SFC program is executed with an AnACPU-F.

5.4 Precautions when Reading/Writing a Program Using a Computer Link

If a microcomputer program (SFC program) of an AnACPU-F is read/written by using a computer link, the following module is unable to execute such a program:

- AD51H intelligent communications module

When a module which is capable of reading/writing a program is utilized, a microcomputer program can be read/written by using a command to read/write a microcomputer program.

5.5 Data Stored to the Status Latch Step Number Storage Register (M9055)

Special register D9055 which is utilized to store a status latch execution step number when status latch is executed is utilized to store the SFC process execution block and step numbers when an SFC program is executed.

- When status latch is executed:
  A status latch execution step number is stored.
  If an SFC program is executed after the execution of status latch, stored data will be overwritten. Therefore, data stored by the execution of status latch must be saved to any other register to avoid overwriting.

- When an SFC program is executed:
  The SFC process execution block and step numbers are stored.

Execution block number (stored in BIN)	Execution step number (stored in BIN)
Higher 8 bits	Lower 8 bits

5.6 Single Start of an Inactive Block

Starting a sub-block other than block 0 requires a sub-block start request issued by any other block in an SFC program.
When an SFC program is executed in an AnACPU-F, any designated block can be started by turning ON the block activating bit of an inactive block by using a program or the test function, etc. of a peripheral device.

(1) How to execute single start of a block
Any of the following methods can be utilized for single start of an inactive block:

- Create a program which turns ON the block activating bit of a block when a condition is established in a sequence program.
- Forcibly turn ON the block activating bit of a block by using the test function of a peripheral device.
- Forcibly turn ON the block activating bit of a block by using a computer link.

(2) Precautions when executing single start of a block
The following precautions must be taken when single start is executed to a designated block:

(a) Each block activating bit needs to be set as a data register in each block.

(b) If the block activating bit of an active block is turned ON by the single start function, the start request is ignored and that block continues execution of an SFC program.

(c) If a sub-block start is executed by an SFC program to a block which has been activated by the single start function, the SFC EXE.ERROR error occurs.
To execute sub-block start by an SFC program, the block activating bit of a corresponding block needs to be included as an interlock in the transition conditions for executing the sub-block start.

(d) Since the block activating bit is turned OFF by the system when the end of the corresponding block has been reached, the user does not need to turn OFF (RST) the bit.
If a block activating bit which is ON is forcibly turned OFF by a sequence program or peripheral device, the end of the corresponding block will not be reached and the block remains active.
In this case, the block activating bit which is included as an interlock for executing a sub-block start by an SFC program is turned OFF, disabling the interlock function. An SFC EXE.ERROR error occurs since a block start request has been made to an already-started block.

6. ERROR CODES WHEN EXECUTING AN SFC PROGRAM

6.1 Error Codes

Table 6.1 lists the messages and codes of the errors that can be caused when executing an SFC program, and the corresponding CPU statuses.

Table 6.1 Error Codes

Error Messages	Error Codes *1	Detail Error Codes *2	CPU statuses		
			Ladders	SFC	
SFC PARA. ERROR	80	801	Continue	Stop	Cannot start the SFC program since the memory cassette is A3(N)MCA-0.
		802			A large enough work area for the SFC program cannot be assigned since the user's memory has free space of 4 Kbytes or less.
		803			The SFC program area in the memory cassette is memory-protected.
		804		Initial start	The memory capacity parameter was changed when continuation restart was designated (M9102: ON).
		805			The CPU was reset when continuation restart was designated (M9102: ON).
SFC CODE ERROR	81	—	Stop	Stop	The SFC program contains an instruction that cannot be decoded.
					After changing the memory capacity parameter, the SFC program capacity became greater than the microcomputer program capacity.
SFC STEP OVER	82	—	Stop	Stop	The number of simultaneous active steps of the SFC program exceeded the maximum (1024).
SFC EXE. ERROR	83	831	Stop	Stop	A request was made to start an active block that was already started.
SFC OPE. ERROR	84	84□ *3	Continue /Stop *4	Continue /Stop *4	An arithmetic operation error occurred. The device range was exceeded when performing an operating output in the SFC program or computing transition conditions using the ladder diagram.

*1: Data register D9008 stores an error code.

*2: Data register D9091 stores a detail error code.

*3: □ indicates the lowest digit of the detail error code (OPERATION ERROR) which occurred when executing the program.
Example:
When data or a constant in a designated device exceeded the allowable range.

Executed Programs	Error Codes	Detail Error Codes
When executing a main program	50	503
When executing an SFC program	84	843

*4: Determined by the error operation mode setting.
The default is "continue".

6.2 Error LED Indicator Priority Setting

This section describes (a) the causes of the errors that light/flash the LED, and (b) the error indication priority.

(1) Error causes that unconditionally light/flash the LED
- When causing an error that stops the CPU.

(2) Error causes (a) whose priority to light/flash the LED can be changed, or (b) that can be set to not to light/flash the LED
The following error causes can be set in special registers D9038 and D9039 to change their priority or to disable light/flash of the LED.

Cause No.	Error Causes	A3A-F	A2A-F
1	Input/Output verification error, fuse blown	Outputs the corresponding error message to the LED display module when an error occurs.	Error LED lit.
2	Special-function module error, link parameter error, operation error, SFC parameter error, SFC operation error		
3	CHK instruction error		
4	Annunciator (F) ON		Error LED flashes.
5	LED instruction		—
6	Battery error		Error LED lit.
7	Clock data		—

7. SFC PROGRAM PROCESSING TIME

This section describes the time required to process a sequence program and an SFC program.

7.1 How to Calculate the Time to Process an SFC Program

This section explains (a) how to calculate the time required to execute an SFC program, and (b) the scan time.

$$\text{Scan time} = \underbrace{\text{time to process a sequence program}}_{1)} + \underbrace{\text{time to process an SFC program}}_{2)} + \underbrace{\text{END processing time}}_{3)}$$

1) Total processing time of instructions used in the main (sub) sequence program.
2) Total of the time of instructions processed for operating output and transition conditions and of system processing.

$$\left(\begin{array}{l}\text{SFC program}\\ \text{processing time}\end{array}\right) = \left(\begin{array}{l}\text{Time of instructions}\\ \text{processed for operating}\\ \text{output and transition conditions}\end{array}\right) + \left(\begin{array}{l}\text{System}\\ \text{processing time}\end{array}\right)$$

(a) Time of instructions processed for operating output and transition conditions

$$\left(\begin{array}{l}\text{Time of instructions}\\ \text{processed for operating}\\ \text{output and transition conditions}\end{array}\right) = \left(\begin{array}{l}\text{Time of instructions}\\ \text{processed for}\\ \text{operating output}\end{array}\right) + \left(\begin{array}{l}\text{Time of instructions}\\ \text{processed for}\\ \text{transition conditions}\end{array}\right)$$

- Operating output instructions processing time
  Total processing time of instructions used for operating output of all executable (active) steps.
  If the transition conditions are satisfied, "total processing time x 2" will be applied.
- Transition condition instructions processing time
  Total processing time of the instructions used for transition conditions included in all executable (active) steps.

(b) System processing time
Section 7.2 gives details about the system processing time and a calculation example.

3) END processing time (self-diagnosis, etc.)

7.2 SFC System Processing Time

This section explains the system processing time (when executing an SFC program) in comparison with the AnNCPU-F.

Table 7.1 SFC System Processing Time

Items		A2ACPU-F	A3ACPU-F	AnNCPU-F
Active-block processing		76.0μs	57.0μs	260.0μs
Inactive-block processing		18.5μs	14.0μs	60.0μs
Available-block processing		5.5μs	4.0μs	60.0μs
Active-step processing		66.5μs	49.5μs	355.0μs
Transition condition processing included in active steps		39.5μs	29.5μs	100.0μs
Transition condition satisfying step processing		22.5μs	17.0μs	60.0μs
SFC END processing	In the case of initial start (M9102: OFF)	38.0μs	28.5μs	285.0μs
	In the case of continuation restart (M9102: ON)	260.0μs	195.0μs	

* SFC system processing time calculation example:
  - Designate continuation restart (M9102: ON)
  - Number of active blocks: 30
    (Active blocks used for an SFC program)
  - Number of inactive blocks: 70
    (Inactive blocks used for an SFC program)
  - Number of available blocks: 50
    (Blocks set by the parameters that are not used for an SFC program)
  - Number of active steps: 60
    (Active steps in active blocks)
  - Transition condition included in active steps: 60
  - Transition condition satisfying steps: 10
    (Active steps that satisfy transition conditions)

SFC system processing time = 195 + (57 x 30) + (14 x 70) + (4 x 50)
+ (49.5 x 60) + (29.5 x 60) + (17 x 10)
= 7795 μs ≈ 8 msec

As indicated above, the SFC system processing time is 8 msec. Under the same conditions, however, it is approx. 11 msec in the case of an A2ACPU-F; approx. 44 msec in the case of an AnNCPU-F. The scan time consists of the SFC system processing time, the time required to process the transition conditions included in the SFC active steps, and the CPU END processing time.

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety inter locking circuit for the PCs.

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(a) Ground human body and work bench.

(b) Do not touch the conductive areas of the printed circuit board and its electrical parts with and non-grounded tools etc.

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<table>
<tr><th rowspan="2">Number</th><th rowspan="2">Name</th><th rowspan="2">Stored Data</th><th rowspan="2">Explanation</th><th colspan="3">Applicable CPU</th></tr>
<tr><th>A1N</th><th>A2N</th><th>A3N</th></tr>
<tr><td>*1D9116
*1D9117
*1D9118
*1D9119
*1D9120
*1D9121
*1D9122
*1D9123</td><td>I/O module verify error</td><td>Bit pattern in modules of 16 points of verify error modules</td><td>• When I/O module data is different from those entered at power-on have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers when parameter setting has been performed.)
<table>
<tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>D9116</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (X/Y0)</td></tr>
<tr><td>D9117</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (X/Y80)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D9123</td><td>0</td><td>1 (X/YF0)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Indicates I/O unit verify error.
(If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)</td><td>●</td><td>●</td><td>●</td></tr>
<tr><td>D9124</td><td>Annunciator detection quantity</td><td>Annunciator detection quantity</td><td>• When one of F0 to 255 is turned on by OUT F□□ or SET F□□, 1 is added to the contents of D9124. When RST F□□ or LED R instruction is executed, 1 is subtracted from the contents of D9124. (For A3NCPU, it can be performed by use of INDICATOR RESET switch on front face of CPU module.)
• Quantity, which has been turned on by OUT F□□ or SET F□□ is stored into D9124 in BIN code. The value of D9124 is maximum 8.</td><td>●</td><td>●</td><td>●</td></tr>
<tr><td>D9125
D9126
D9127
D9128
D9129
D9130
D9131
D9132</td><td>Annunciator detection number</td><td>Annunciator detection number</td><td>• When one of F0 to 255 is turned on by OUT F□□ or SET F□□, F number, which has turned on, is entered into D9125 to D9132 in due order in BIN code.
• F number, which has been turned off by RST F□□, is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the preceding data registers.
• By executing LED R instruction, the contents of D9125 to D9132 are shifted upward by one. (For A3NCPU, it can be performed by use of INDICATOR RESET switch on front of CPU unit.)
• When there are 8 annunciator detections, the 9th one is not stored into D9125 to 9132 even if detected.
<table>
<tr><th></th><th>SET F50</th><th>SET F25</th><th>SET F19</th><th>RET F25</th><th>SET F15</th><th>SET F70</th><th>SET F65</th><th>SET F38</th><th>SET F110</th><th>SET F151</th><th>SET F210</th><th>LED R</th></tr>
<tr><td>D9009</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td></tr>
<tr><td>D9124</td><td>0</td><td>1</td><td>2</td><td>3</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>8</td><td>8</td></tr>
<tr><td>D9125</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td></tr>
<tr><td>D9126</td><td>0</td><td>0</td><td>25</td><td>25</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>15</td></tr>
<tr><td>D9127</td><td>0</td><td>0</td><td>0</td><td>99</td><td>0</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>70</td></tr>
<tr><td>D9128</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>65</td></tr>
<tr><td>D9129</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>65</td><td>65</td><td>65</td><td>65</td><td>65</td><td>38</td></tr>
<tr><td>D9130</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>38</td><td>38</td><td>38</td><td>38</td><td>110</td></tr>
<tr><td>D9131</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>110</td><td>110</td><td>110</td><td>151</td></tr>
<tr><td>D9132</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>151</td><td>151</td><td>210</td></tr>
</table></td><td>●</td><td>●</td><td>●</td></tr>
</table>

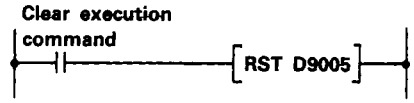
Special Register List

POINT

(1) All special register data is cleared by any of the power-off, latch clear and reset operations. The data is retained when the RUN/STOP switch is set to STOP.

(2) For the above special registers with numbers marked *1, the contents of register are not cleared if normal status is restored. Therefore, to clear the contents, use the following method:

1) Method by user program.



Insert the circuit shown at right into the program and turn on the clear execution command contact to clear the contents of register.

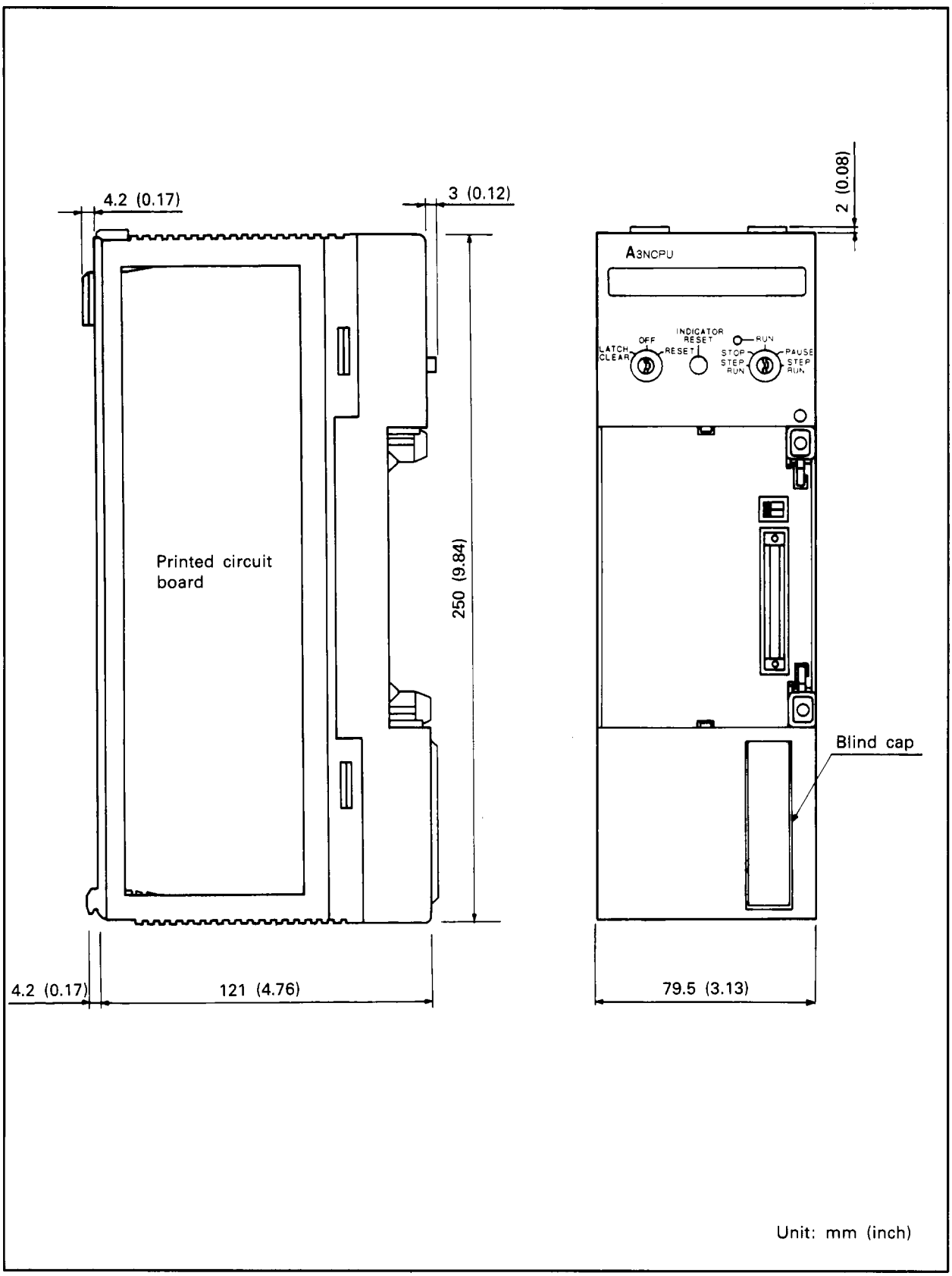
2) Method by peripheral equipment.
Set the register to "0" by changing the present value by the test function of peripheral equipment or set to "0" by forced reset. For the operation procedure, refer to the manual of each peripheral equipment.

3) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

(3) Data is written to the special registers marked *2 by the sequence program.

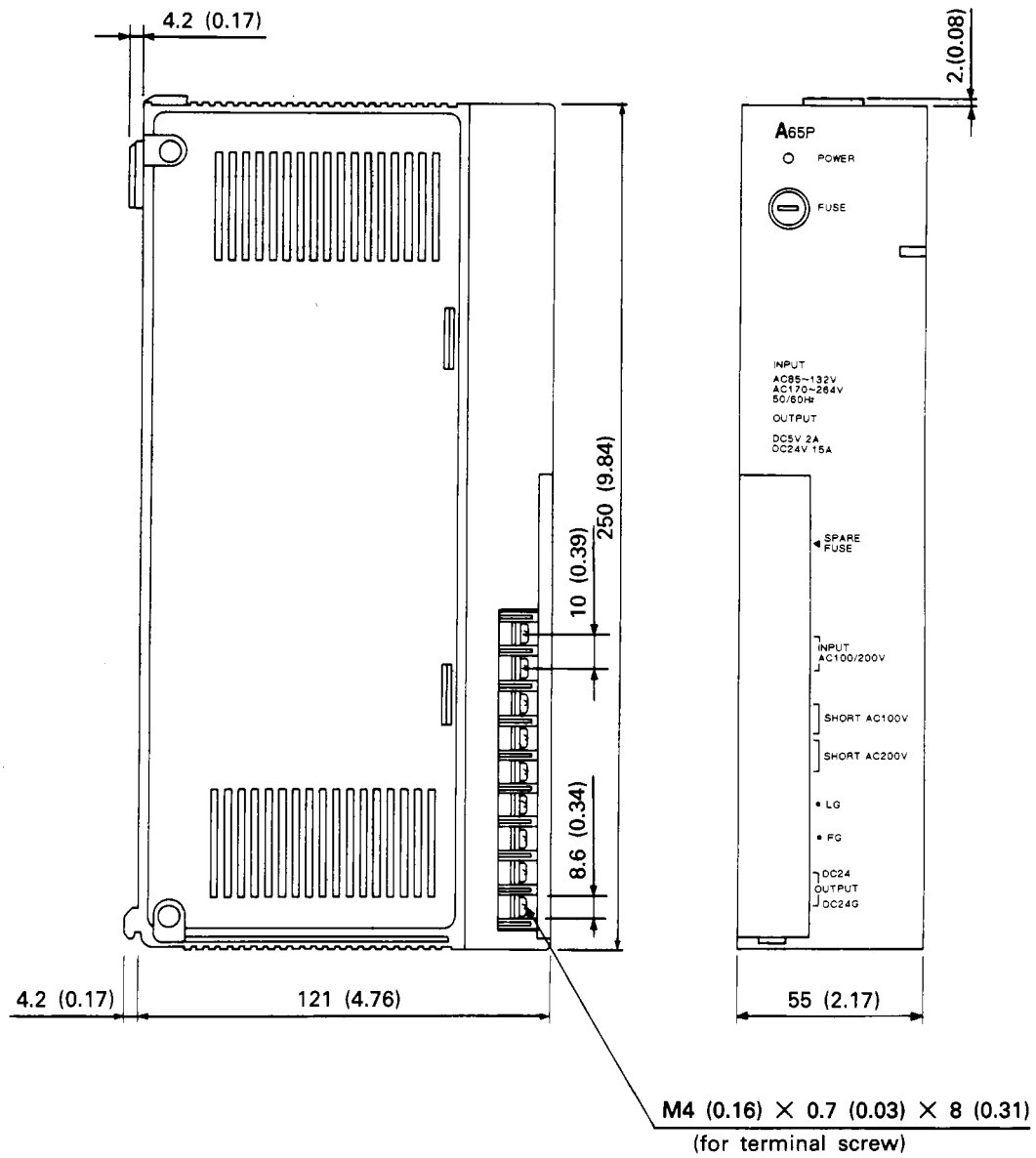
APPENDIX 4 Dimensions

4.1 CPU module



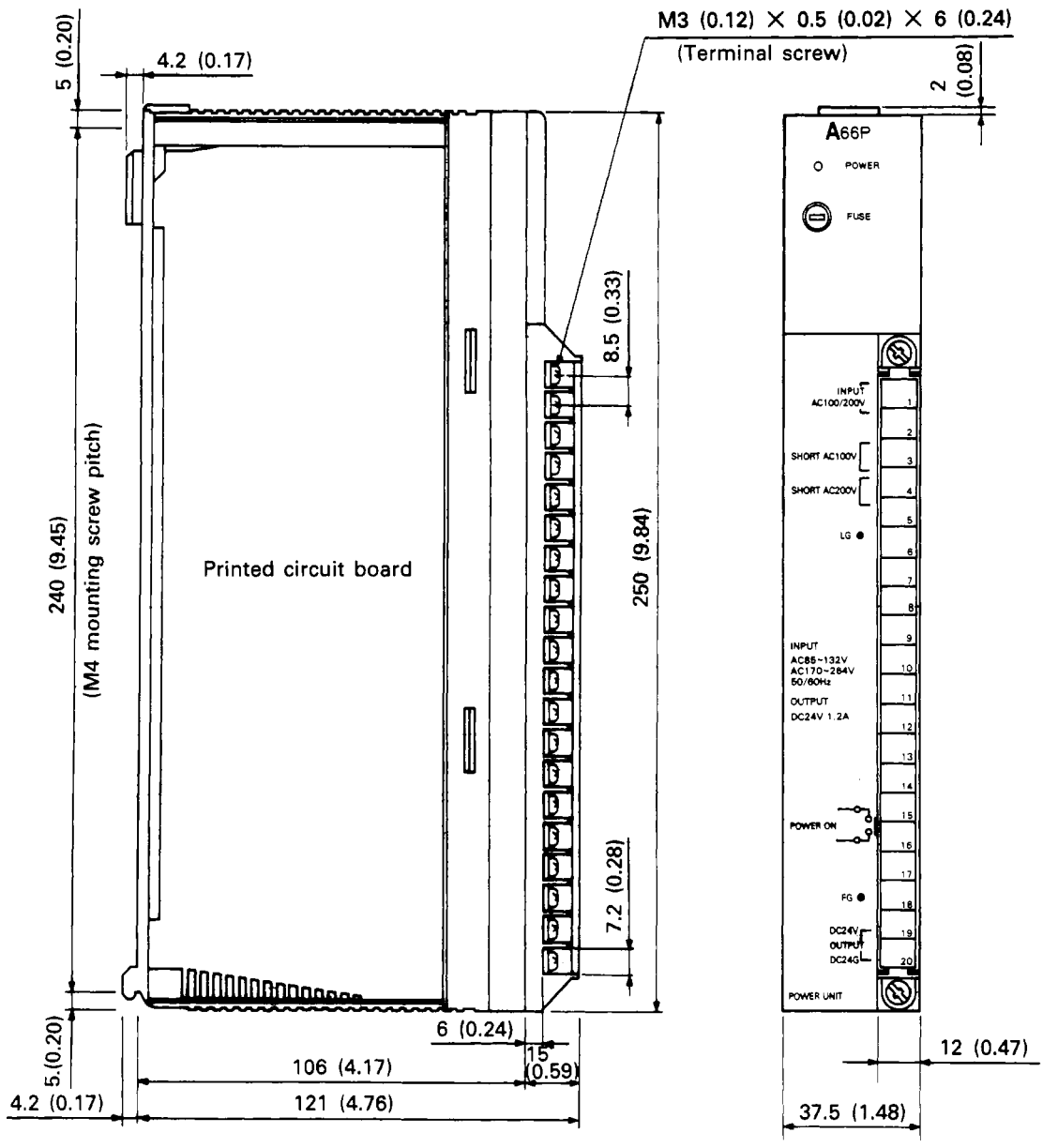
4.2 Power supply modules

(1) Type A61P, A62P, A63P, A65P power supply modules



Unit: mm (inch)

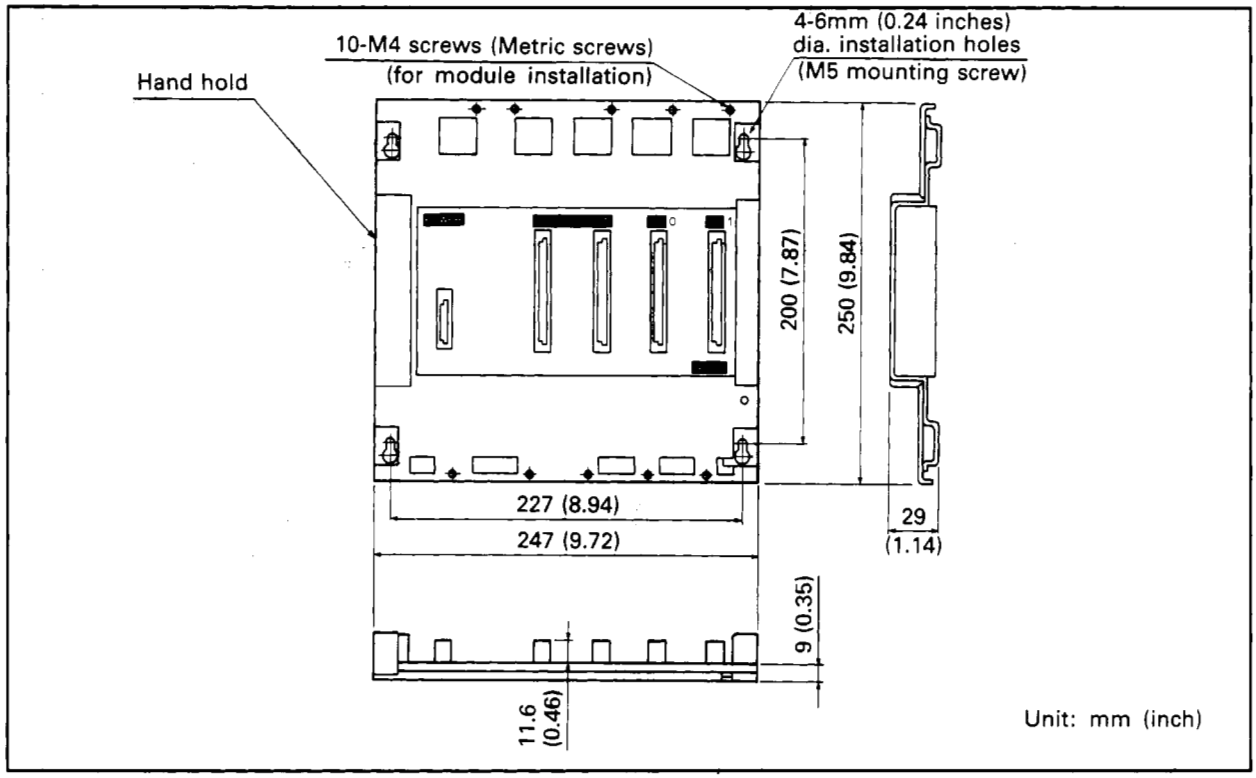
(2) Type A66P power supply module



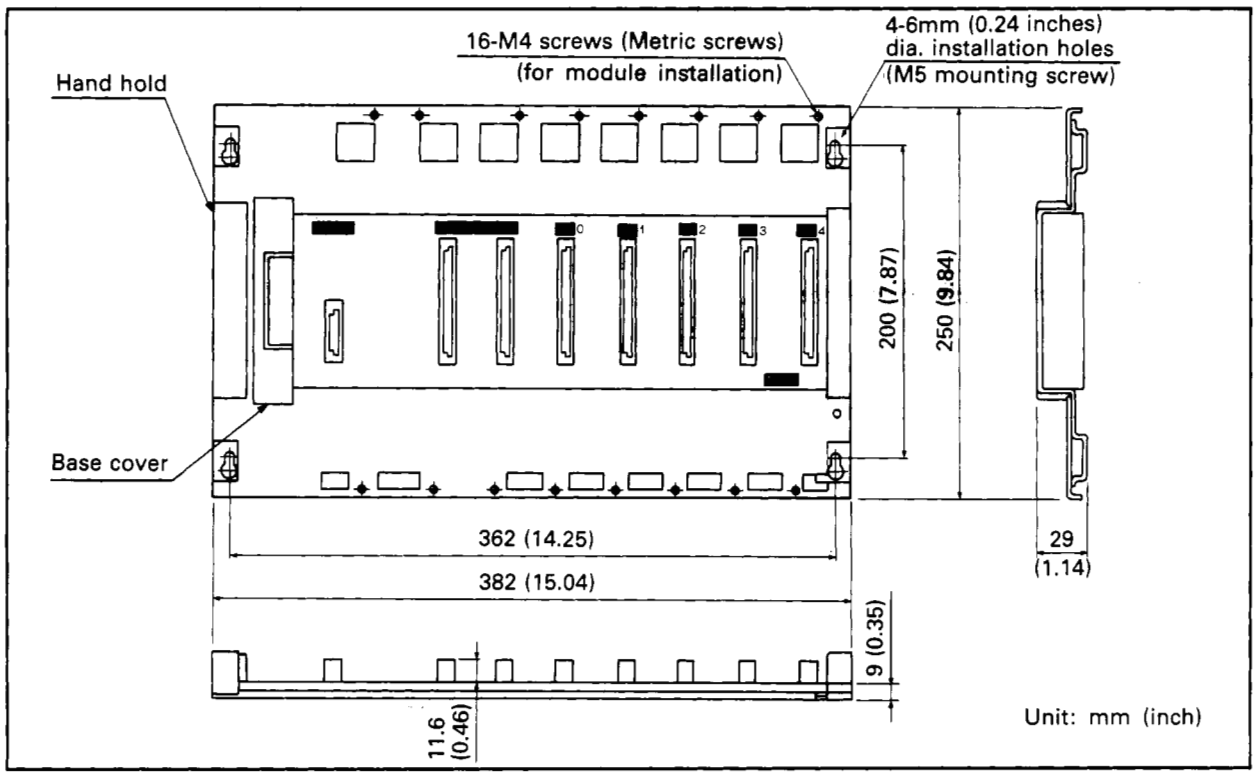
Unit: mm (inch)

4.3 Basic base units

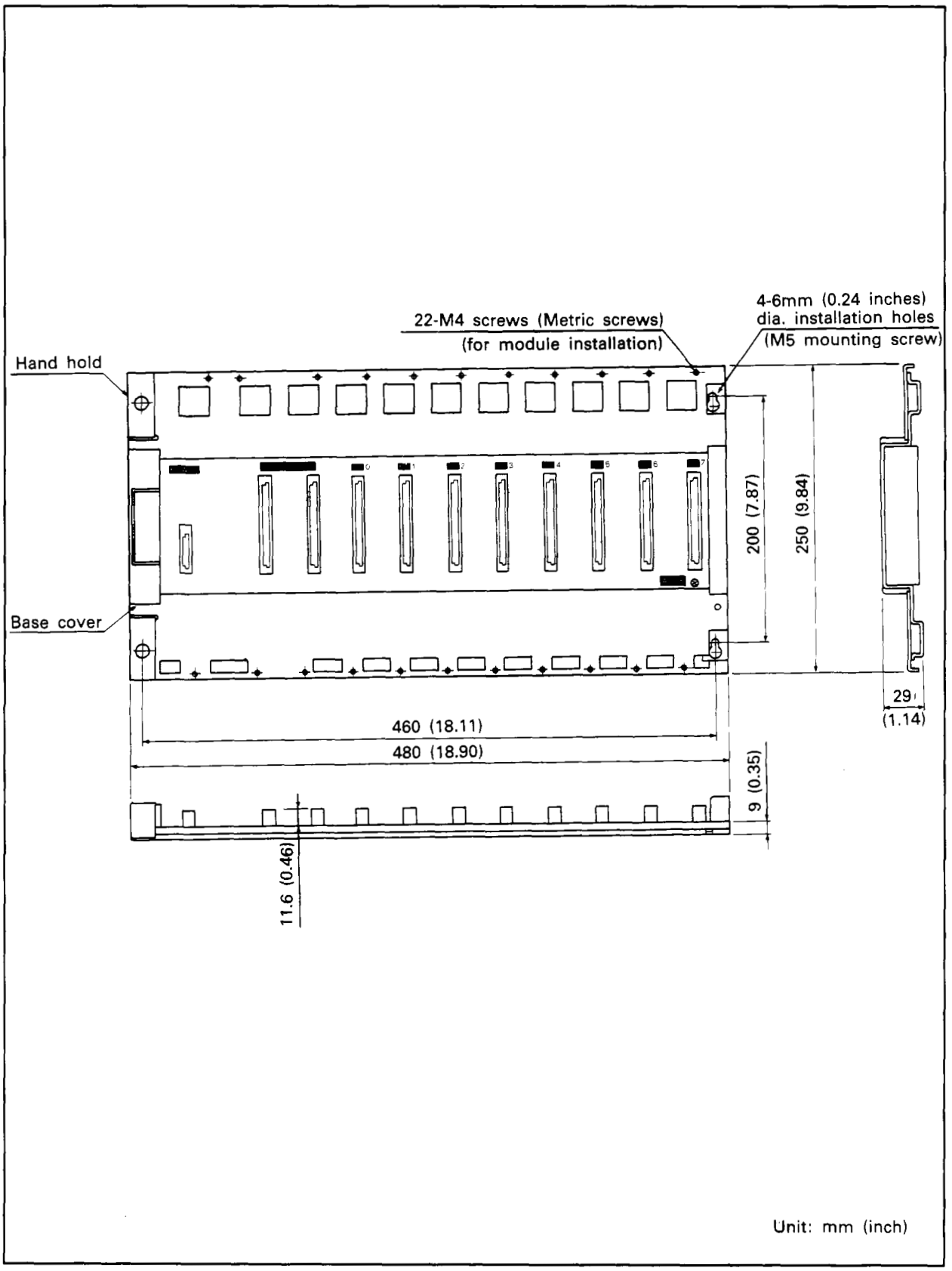
(1) Type A32B base unit



(2) Type A35B base unit

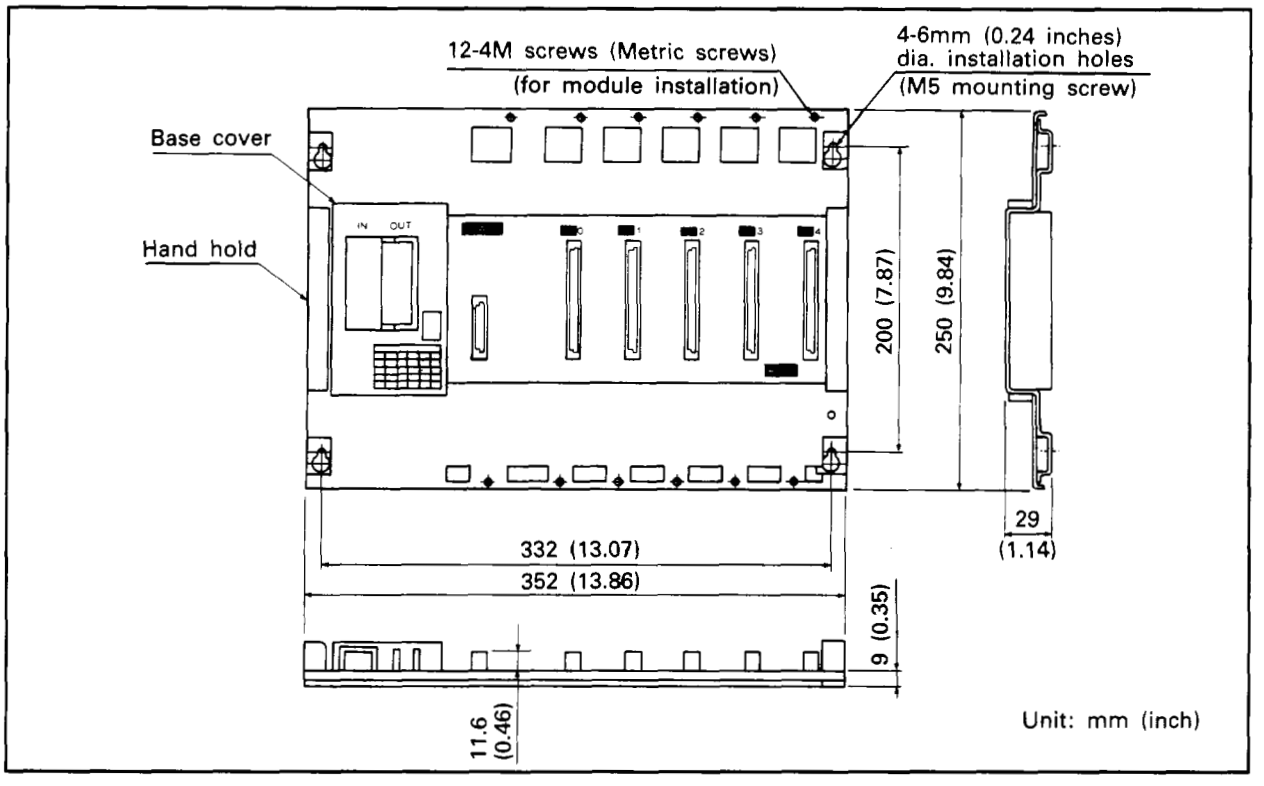


(3)Type A38B base unit

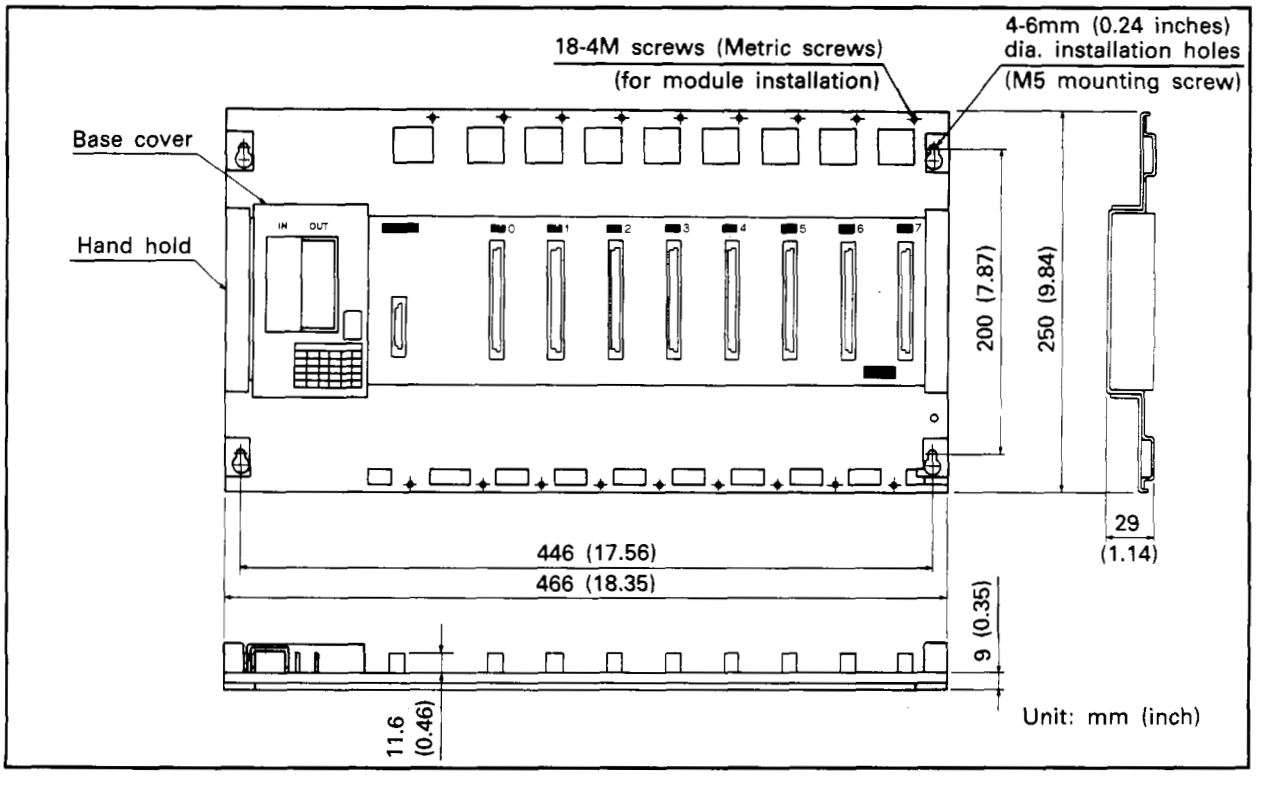


4.4 Extension base units

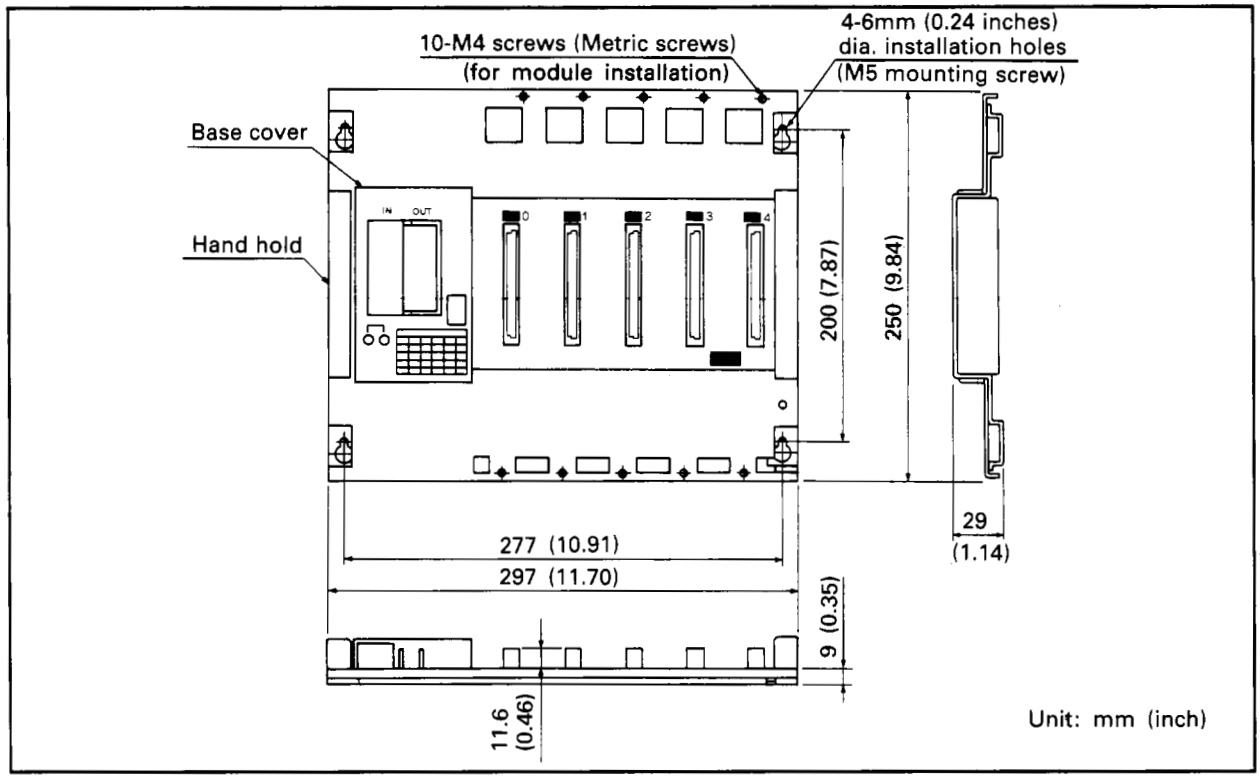
(1) Type A65B base unit



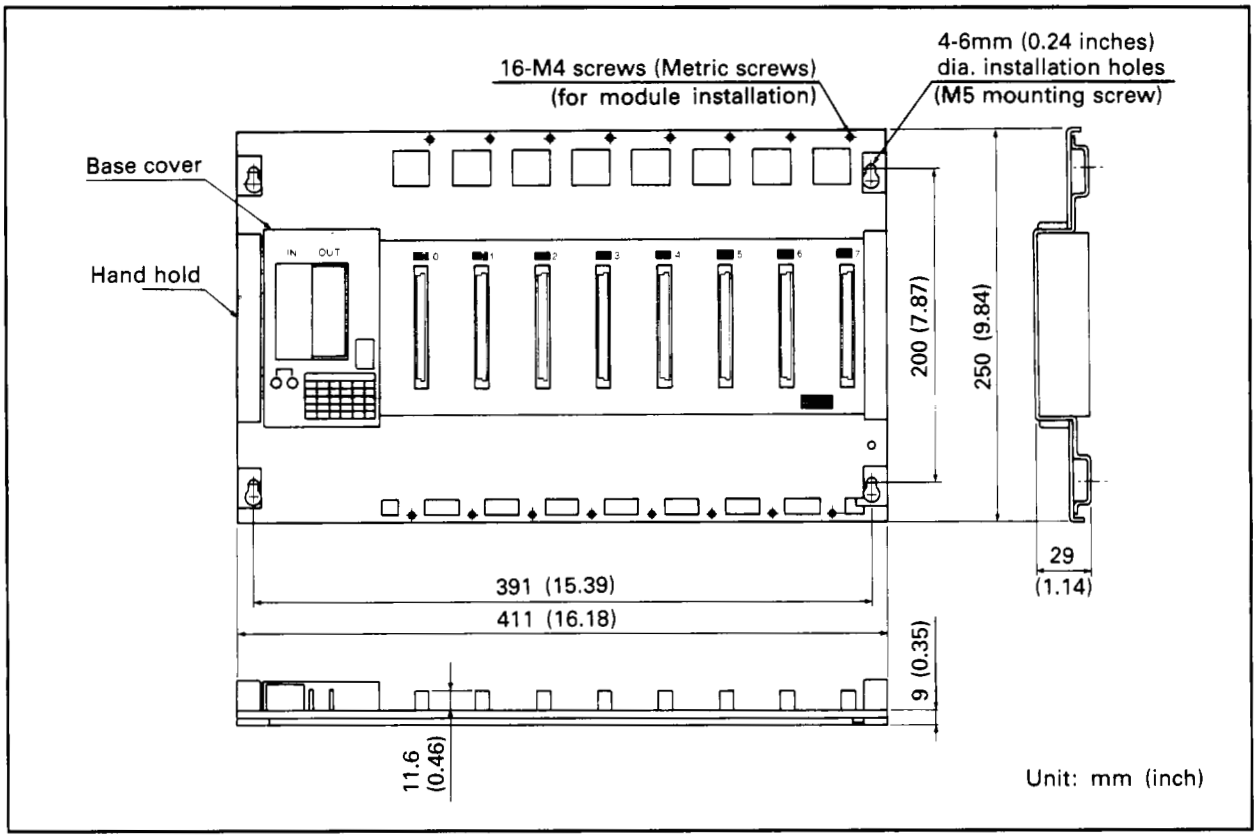
(2) Type A68B base unit



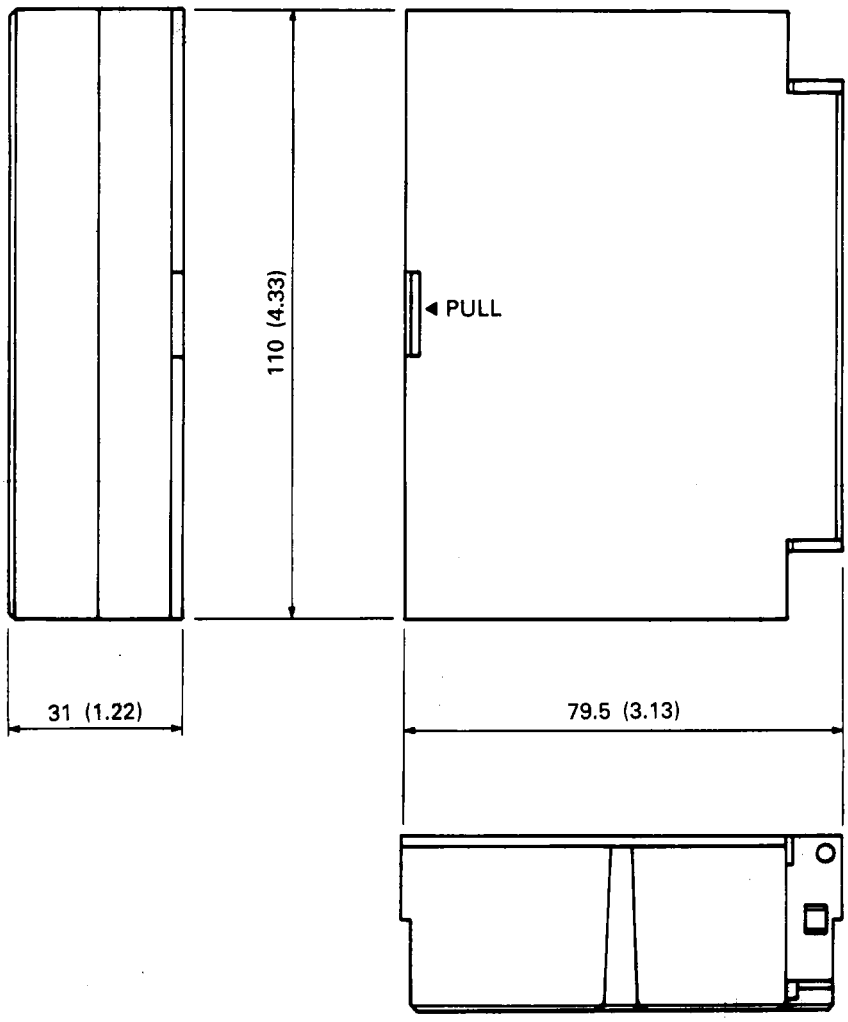
(3) Type A55B base unit



(4) Type A58B base unit



4.5 Memory cassettes (A3NMCA-□)



Unit: mm (inch)

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety inter locking circuit for the PCs.

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(a) Ground human body and work bench.

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Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

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